AMENDMENTS TO THE SPECIFICATION:

Please delete the heading beginning at page 1, line 1, which starts with:

BACKGROUND OF THE...

Please amend the heading beginning at page 2, line 1, as follows:

Summary ~~of the Invention~~

Please amend the paragraph beginning at page 2, line 16, as follows:

The present ~~invention recognises~~ inventors recognized that during the operation of many data processing apparatus, the probability that a data transfer will occur between a master logic unit and a slave logic unit pair over the bus without the bus being requested for use by other logic unit pairs is statistically relatively high. Hence, for the majority of data transfers it is accurate to assume that the data transfer will occur with exclusive access to the bus. Assuming that each data transfer can occur with exclusive access to the bus significantly decreases the complexity when generating the anticipated timing information for each data transfer. The complexity is decreased because the need to precisely model the generation of signals used to request the bus by every logic unit in the data processing apparatus is obviated. Furthermore, the complexity is decreased because there is no need to precisely model the operation of any bus arbitration logic responsive to those signals. Accordingly, because the complexity of the model which generates the anticipated timing information can be low, the speed at which the anticipated timing information is generated is high. Also, because the majority of the data transfers will in fact occur under these conditions, the majority of the anticipated timing information will be accurate.

Please delete the paragraph beginning at page 7, line 24, which starts with:

The present invention will…

Please amend the heading beginning at page 8, line 7, as follows:

Detailed Description ~~of the Preferred Embodiments~~